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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/394,302	09/10/1999	ALVAR A. DEAN	BU9-98-062	4030

29154 7590 06/18/2003

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EXAMINER
CHU, GABRIEL L

ART UNIT	PAPER NUMBER
2184	11

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/394,302	Applicant(s) DEAN ET AL.	
	Examiner Gabriel L. Chu	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *55-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *55-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *11* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 55-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. Referring to claim 55, Steiner discloses a transportable circuit chip test device comprising: a transportable test box (See figure 1.); a test board in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards (From the abstract, "A battery operated..."), wherein said test board comprises: a socket adapted to hold integrated circuit chips to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.). Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one

integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time".

Referring to claim 56, Steiner in combination with Miller et al. disclose each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13 so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of tests which will test all the relevant combinations of inputs for the unit under test and tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the UUT failed the test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures. External documentation of the testing procedures can identify the particular input/output combination for which the unit under test failed to respond properly if this is considered important to the user.").

Referring to claim 57, Steiner in combination with Miller et al. disclose the portable power supply comprises a battery (From the abstract of Steiner, "A battery operated...").

Referring to claim 58, Steiner in combination with Miller et al. disclose each of said test boards includes a memory adapted to store test results (From line 54 of

column 4 of Miller et al., "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

Referring to claim 59, Steiner in combination with Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

Referring to claim 60, Steiner in combination with Miller et al. disclose each of said test boards includes comparators electrically connected to said sockets (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

Referring to claim 61, Steiner in combination with Miller et al. disclose said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in

each of a number of devices under test (DUTs)."), and wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

Referring to claim 62, Steiner in combination with Miller et al. disclose said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously (From the technical field of Miller et al., "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel.").

Referring to claim 63, Steiner discloses a transportable integrated circuit (IC) chip test device, said device comprising: a transportable test box (See figure 1.); a test board mounted in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards (From the abstract, "A battery operated..."), wherein said test board comprises: sockets adapted to hold an IC chip to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.). Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well

known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time". Further, although Steiner does not specifically disclose the comparison of a plurality of ICs, it is known in the art. An example of this is further shown by Miller et al. Miller et al. disclose said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said IC chips simultaneously, and wherein said testing circuitry identifies a defective IC chip as one having a different output when compared to outputs of the other ASIC chips, when all IC chips are supplied with identical inputs (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from the abstract, "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD." Further, from

the technical field, "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel." Wherein a faulty circuit's output is different.). A person of ordinary skill in the art at the time of the invention would have been motivated to compare DUTs in a portable tester because, from line 24 of column 1, "the manufacturer expects each constituent IC device to be virtually free of defects and to perform according to its specifications." Further, although Steiner does not specifically disclose the test device is adapted to test application specific integrated circuits (ASICs), the testing of ICs that are application specific is well known in the art. An example of this is an ASIC tester. A person of ordinary skill in the art at the time of the invention would have been motivated to test ASICs because they can be faulty.

Referring to claim 64, Steiner in combination with Miller et al. disclose all of said ASIC chips have an identical design (From line 6 of column 3, "As briefly summarized above, an embodiment of the invention provides for more efficient testing of a number of similar, and preferably identical, IC devices in parallel without altering the test program or the conventional tester.").

Referring to claim 65, Steiner in combination with Miller et al. disclose each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13 so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of

tests which will test all the relevant combinations of inputs for the unit under test and tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the UUT failed the test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures. External documentation of the testing procedures can identify the particular input/output combination for which the unit under test failed to respond properly if this is considered important to the user.").

Referring to claim 66, Steiner in combination with Miller et al. disclose the portable power supply comprises a battery (From the abstract of Steiner, "A battery operated...").

Referring to claim 67, Steiner in combination with Miller et al. disclose each of said test boards includes a memory adapted to store test results (From line 54 of column 4 of Miller et al., "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

Referring to claim 68, Steiner in combination with Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester

communicates with a known good device through a channel.").

Referring to claim 69, Steiner in combination with Miller et al. disclose all of said comparators are connected to known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs). The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

3. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. as applied to claim 63 above, and further in view of US 6499121 to Roy et al. Referring to claim 70, although Steiner in combination with Miller et al. do not specifically disclose by comparing whether outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested, testing without a known output is known in the art. An example of this is given by Roy et al. in line 13 of column 2, "Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors on each channel are fanned out to multiple DUTs.

In general, the test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If desired, the interface circuitry may be further enhanced with error detection capability based on the responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form." Further, from line 55 of column 6, "The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in relation to FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the interface circuitry 226 performs cross-DUT

and within-DUT comparisons, such as in FIGS. 7-9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology." A person of ordinary skill in the art at the time of the invention would have been motivated to incorporate the teachings of Roy et al. into a portable circuit tester because, from line 8 of column 7, it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7, "[e]liminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology."

Allowable Subject Matter

4. The indicated allowability of claims 55-70 is withdrawn in view of the newly discovered reference(s) to US 4291404 to Steiner, US 6452411 to Miller et al., and US 6499121 to Roy et al. Rejections based on the newly cited reference(s) follow.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 4559626 to Brown

US 4639664 to Chiu et al.

US 5243274 to Kelsey et al.

US 6031386 to Cole, Jr. et al.

US 6055653 to LeBlanc et al.

US 6112163 to Oowaki et al.

US 6195616 to Reed et al.

US 6198273 to Onishi et al.

US 6476628 to LeColst

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

gc
June 12, 2003

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